**Institute of Engineering & Management**

**Department of Computer Science & Engineering**

**Computer Architecture Laboratory for 2nd year 4th semester 2018**

**Code: CS 493**

**Date:** 17/02/18

**WEEK-3**

**Assignment-1:** Implementation of 8 bit Adder, 8 bit Subtractor, 8 bit Parallel Adder, 8 bit

Parallel Subtractor, 4 bit Multiplier & 8 bit Comparator using Xilinx ISE.

**Objective:** To implement 8 bit Adder

**Software used:**

|  |  |
| --- | --- |
| Property Name | Value |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
3. Make test bench waveform and check for the given inputs.

**Data flow Model:**

**Data flow Model Code:**

entity a1 is

Port ( a : in STD\_LOGIC\_VECTOR (7 downto 0);

b : in STD\_LOGIC\_VECTOR (7 downto 0);

c : out STD\_LOGIC\_VECTOR (7 downto 0));

end a1;

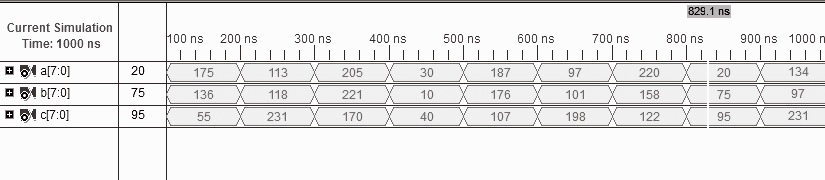
architecture Behavioral of a1 is

begin

c<=a+b;

end Behavioral;

**Output:**



**Objective:** To implement 8 bit subtractor

**Software used:**

|  |  |
| --- | --- |
| Property Name | Value |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.

iii. Make test bench waveform and check for the given inputs.

**Data flow Model:**

**Data flow Model Code:**

entity a1 is

Port ( a : in STD\_LOGIC\_VECTOR (7 downto 0);

b : in STD\_LOGIC\_VECTOR (7 downto 0);

c : out STD\_LOGIC\_VECTOR (7 downto 0));

end a1;

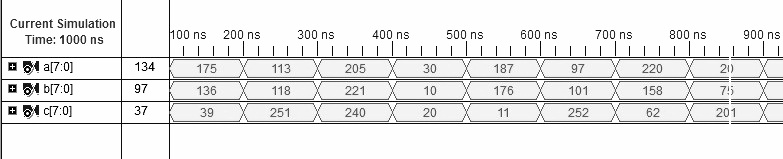
architecture Behavioral of a1 is

begin

c<=ab;

end Behavioral;

**Output:**



**Objective:** To implement 8 bit Comparator

**Software used:**

|  |  |
| --- | --- |
| Property Name | Value |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
3. Make test bench waveform and check for the given inputs.

**Data flow Model:**

**Data flow Model Code:**

entity a3 is

Port ( a : in STD\_LOGIC\_VECTOR (7 downto 0);

b : in STD\_LOGIC\_VECTOR (7 downto 0);

low : out STD\_LOGIC;

high : out STD\_LOGIC;

equal : out STD\_LOGIC);

end a3;

architecture Behavioral of a3 is

begin process(a,b)

begin

if (a<b) then

low<='1';

high<='0';

equal<='0';

elsif (a>b) then

low<='0';

high<='1';

equal<='0';

elsif (a=b) then

low<='0';

high<='0';

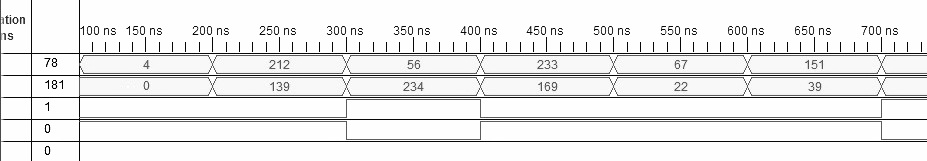
equal<='1';

end if;

end process;

end Behavioral;

**Output:**



**Objective:** To implement 8 bit Parallel Adder

**Software used:**

|  |  |
| --- | --- |
| Property Name | Value |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.

iii. Make test bench waveform and check for the given inputs.

**Data flow Model:**

**Data flow Model Code:**

entity a2 is

Port ( a : in STD\_LOGIC\_VECTOR (7 downto 0);

b : in STD\_LOGIC\_VECTOR (7 downto 0);

cin : in STD\_LOGIC;

s : out STD\_LOGIC\_VECTOR (7 downto 0));

end a2;

architecture Behavioral of a2 is

begin process(a,b,cin)

variable ct:std\_logic\_vector(7 downto 0);

begin

ct(0):=cin;

for i in 0 to 7 loop

s(i)<=a(i) xor b(i) xor ct(i);

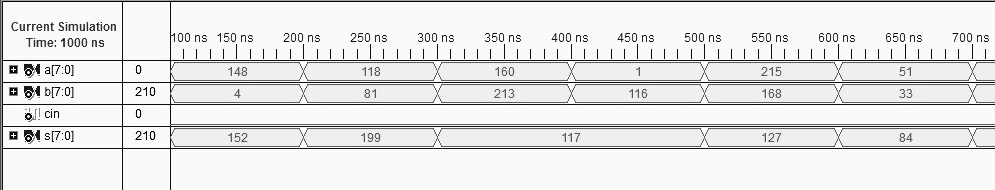
ct(i+1):=( a(i) and b(i)) or (b(i) and ct(i)) or (a(i) and ct(i));

end loop;

end process;

end Behavioral;

**Output:**



**Objective:** To implement 8bit Parallel Subtractor

**Software used:**

|  |  |
| --- | --- |
| Property Name | Value |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.
3. Make test bench waveform and check for the given inputs.

**Data flow Model:**

**Data flow Model Code:**

entity a2 is

Port ( a : in STD\_LOGIC\_VECTOR (7 downto 0);

b : in STD\_LOGIC\_VECTOR (7 downto 0);

cin : in STD\_LOGIC;

s : out STD\_LOGIC\_VECTOR (7 downto 0));

end a2;

architecture Behavioral of a2 is

begin process(a,b,cin)

variable ct:std\_logic\_vector(7 downto 0);

begin

ct(0):=cin;

for i in 0 to 7 loop

s(i)<=a(i) xor b(i) xor ct(i);

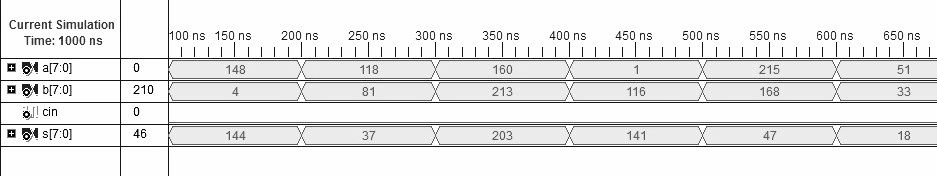
ct(i+1):=((not a(i)) and b(i)) or (b(i) and ct(i)) or ((not a(i)) and ct(i));

end loop;

end process;

end Behavioral;

**Output:**



**Objective:** To implement 4bit Multiplier

**Software used:**

|  |  |
| --- | --- |
| Property Name | Value |
| Device family | Spartan 3 |
| Device | XC3S50 |
| Package | PQ208 |
| Speed | -5 |
| Top-level source type | HDL |
| Synthesis Tool | XST(VHDL/Verilog) |
| Simulator | ISE Simulator |
| Preferred Language | VHDL |

**Theory:**

1. Make VHDL with required port specification.
2. Calculate the value c for both data flow and behavioral model using if and else statement with required condition.

iii. Make test bench waveform and check for the given inputs.

**Data flow Model:**

**Data flow Model Code:**

entity a4 is

Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);

b : in STD\_LOGIC\_VECTOR (3 downto 0);

c : out STD\_LOGIC\_VECTOR (7 downto 0));

end a4;

architecture Behavioral of a4 is

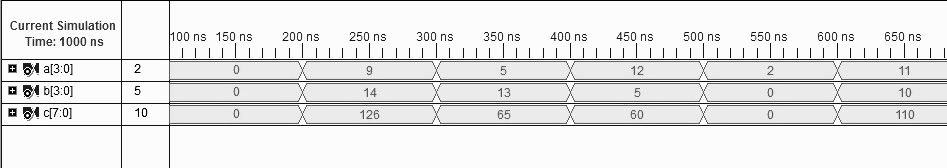
begin process(a,b)

begin

c<=a\*b;

end process;

end Behavioral;

**Output: **